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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO.
09/888,494	06/26/2001	Han-Chao Lai	4425-154	9082

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EXAMINER	
PHAM, LONG	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,494	LAI ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1 136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (US006130454A) and Hsu et al. (US006221767B1).

Gardner teaches a method of forming a MOSFET, said method comprises (see figures 1-2, 3a-3b, 4-8, 9a-9b, 10a-10b, and 11-12 and col. 1, line 5 to col. 9, line 30):

providing a wafer, wherein said wafer comprises a substrate 10;

forming a trench 20 in said substrate;

forming a gate 40 on a bottom of said trench;

forming a spacer 46 on both sides of said gate and filling of said trench;

implanting an ion into said substrate which is on both sides of said spacer;

proceeding a first thermal process to form a source/drain region 50 and a source/drain extended region 48 in said substrate;

forming a metal layer on said gate, said spacer, and said source/drain region (see figure 12 and 8, lines 59-67);

proceeding a second thermal process to form a silicide layer on said gate and said source/drain region.

Gardner teaches that the activation of source/drain implanted ions is done by heating, but fails to teach the activation of source/drain implanted ions is done by rapid heating as recited in present claim 1.

However, it is well-known to one skilled in the art that rapid heating has been used in activating ion implanted region because rapid heating reduces the unwanted heat exposure to the device.

Gardner fails to explicitly teach the removal of unreacted metal after the silicidation process as recited in present claim 1.

Hsu teaches that the unreacted metal that is formed during the silicidation process is removed. See col. 3, lines 24-37.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to incorporate Hsu's above teaching into Gardner's method because in doing so a silicide layer having low resistance can be obtained. See col. 3, lines 24-37.

With respect to claim 2, Gardner teaches the gate comprises of a gate oxide layer 36. See figure 6.

With respect to claims 4 and 5, Gardner teaches that the ion is of n or p. See co. 8, lines 20-30.

With respect to claims 6 and 7, Gardner teaches that the metal layer is made of titanium or cobalt. See col. 8, lines 60-65.

Gardner fails to teach that platinum is used in forming the silicide as recited in present claim 8.

However, it is well-known to one skilled in the art that platinum is used as metal in forming silicide.

Gardner fails to teach that the depth of the trench is about 50 to 80 percent of a thickness of the gate as recited in present claim 3.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal range for the depth of the trench relative to the thickness of the gate through routine experimentation and optimization to obtain optimal or desired device performance because the depth of the trench is a result-effective variable and there is no evidence indicating that the depth of the trench is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable

within given prior art conditions by routine experimentation. See MPEP 2144.05.

2. Claims 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (US006130454A) and Hsu et al. (US006221767B1) and Brigham et al. ('413).

Gardner teaches a method of forming a MOSFET, said method comprises (see figures 1-2, 3a-3b, 4-8, 9a-9b, 10a-10b, and 11-12 and col. 1, line 5 to col. 9, line 30):

providing a wafer, wherein said wafer comprises a substrate 10;

forming a trench 20 in said substrate;

forming a gate 40 on a bottom of said trench, wherein said gate comprises a gate oxide layer;

forming a spacer 46 on both sides of said gate and filling of said trench;

implanting an ion into said substrate which is on both sides of said spacer;

proceeding a first thermal process to form a source/drain region 50 and a source/drain extended region 48 in said substrate;

forming a metal layer on said gate, said spacer, and said source/drain region (see figure 12 and 8, lines 59-67);

proceeding a second thermal process to form a silicide layer on said gate and said source/drain region.

Gardner teaches that the activation of source/drain implanted ions is done by heating, but fails to teach the activation of source/drain implanted ions is done by rapid heating as recited in present claim 9.

However, it is well-known to one skilled in the art that rapid heating has been used in activating ion implanted region because rapid heating reduces the unwanted heat exposure to the device.

Gardner fails to teach that the silicide layer is formed by two rapid thermal treatments and the unreacted metal is removed as recited in present claim 9. Hsu teaches a silicide layer is formed by two rapid thermal treatments and the unreacted metal is removed. See col. 3, lines 24-37.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to incorporate Hsu's above teaching into Gardner's method because in doing so a silicide layer having low resistance can be obtained. See col. 3, lines 24-37.

With respect to claims 11 and 12, Gardner teaches that the ion is of n or p. See co. 8, lines 20-30.

With respect to claims 13 and 14, Gardner teaches that the metal layer is made of titanium or cobalt. See col. 8, lines 60-65.

Gardner fails to teach that platinum is used in forming the silicide as recited in present claim 15.

However, it is well-known to one skilled in the art that platinum is used as metal in forming silicide.

Gardner fails to teach that the depth of the trench is about 50 to 80 percent of a thickness of the gate as recited in present claim 10.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal range for the depth of the trench relative to the thickness of the gate through routine experimentation and optimization to obtain optimal or desired device performance because the depth of the trench is a result-effective variable and there is no evidence indicating that the depth of the trench is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable

within given prior art conditions by routine experimentation. See MPEP 2144.05.

Gardner fails to teach the range of the temperature for the activation of source/drain as recited in present claim 17.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal range of the temperature for the activation of source/drain through routine experimentation and optimization to obtain optimal or desired device performance because the temperature for the activation of source/drain is a result-effective variable and there is no evidence indicating that the temperature for the activation of source/drain is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Gardner fails to teach range of the width of the trench as recited in present claim 18.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal range for width of the trench through routine experimentation and optimization to obtain optimal or desired device performance because the width of the trench is a result-effective variable and there is no evidence indicating that the width of the trench is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Gardner teaches that the spacer is made of oxide, but fails to teach that the spacer is made of nitride as recited in present claim 16.

Brigham teaches that nitride is used as spacer. See col. 5, lines 16-27.

It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to use nitride spacer in Gardner's method because nitride has better hermeticity. See col. 5, lines 16-27.

Response to Arguments

In response to the applicant's arguments in the paragraph connecting pages 4 and 5, the first paragraph of page 5, and the paragraph connecting pages 5 and 6 of the Amendment dated 10/09/02, it is submitted that layer 46 is being referenced to as the spacer not layer 32 in Gardner et al. (US006130454A). Further, it is submitted that claims 1-18 do not preclude the formation of nitride layer 16 because of the recitation of "comprises" in the preamble of the claims 1-18.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Long Pham
Primary Examiner
Art Unit 2814

L. P.

June 26, 2003